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Design and Implementation of Cascade H Bridge Multilevel Inverter

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ABSTRACT: In this paper main focus is on the design and implementation of a new topology in a single phase seven level cascaded H-bridge multilevel inverter by using only a seven switches and two DC power source. The main objective of this paper is to increase number of levels with a low number of switches and sources at the output without adding any complexity to the power circuit. The main merit of the new topology is to reduce the lower total harmonic distortion, lower electromagnetic interference generation and high output voltage. In this paper, various carrier pulse width modulation techniques are proposed, which can minimize the total harmonic distortion and enhances the output voltages from proposed work of seven level inverter. The various switching topologies of single-phase seven level cascaded H-bridge multilevel inverters have been analyzed in this paper. The simulation is done by Mat Lab 8.0 version software. [1] The control signals for power electronic switches are provided using different pulse width modulation modulated technique. Harmonic analysis carried out using Mat Lab 8.0 version software .It is proved that proposed work of Single phase seven level multilevel cascade inverter output voltage total harmonics distortion is reduced and improve the efficiency of system compare with different topologies of single phase seven level multilevel cascade inverter.

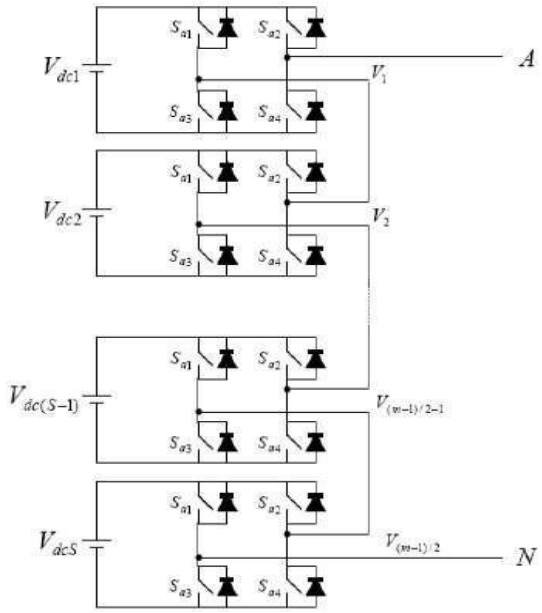


Fig 1.1: Equivalent circuit of Cascaded Multilevel inverter[1].

This paper aims to extend the knowledge about the performance of five levels Cascaded H-Bridge MLI topology with DC/DC Boost Converter using SPWM for fixed DC Source. The output voltage is the sum of the voltage that is generated by each bridge. The switching angles can be chosen in such a way that the total harmonic distortion is minimized. This topology incorporates Boost Converter in the input side which magnifies the fundamental output voltage with reduction in total harmonic distortion.
It also incorporates LC filter and hence output is drawn near the sine wave because of more levels. The performance of the proposed SPWM strategy in terms of output voltage and THD has studied successfully and shown using MATLAB/Simulink. The design of the 7-level multilevel inverters seems to be better than the 9-level multilevel inverters. By increasing the number of levels, the cost and weight of the multilevel inverter will be increased. So this topology is well suited for industrial drives.

The multilevel inverter utilization has been increased since the last decade. These new type of inverters are suitable in various high voltage and high power applications due to their ability to synthesize waveforms with better harmonic spectrum and faithful output. This paper presents an asymmetrical seven level cascaded H-bridge multilevel inverter, using multicarrier pulse width modulation technique[2]. And also comparison is made between multicarrier pulse width modulation and the embedded mat lab function. This topology also reduces the number of switches and also the cost. From the results, the proposed inverter provides higher output quality with relatively lower power loss as compared to the other conventional inverters with the same output quality. [4] In this paper, the simulation results show that the total harmonic distortion is low for multicarrier modulation method. The total harmonic distortion can be further reduced by using filter circuit. This circuit also reduces the number of switches and sources.

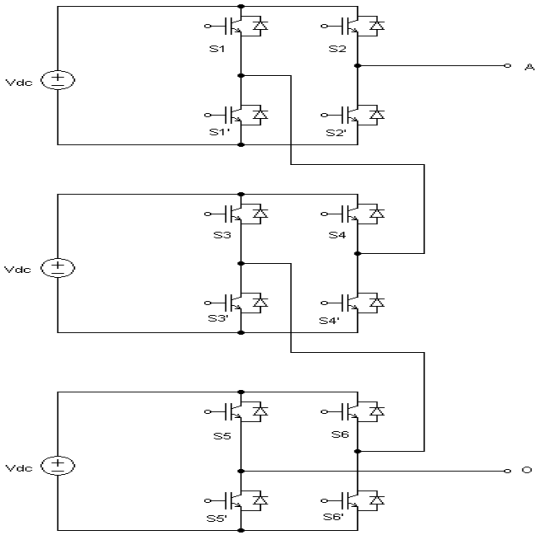


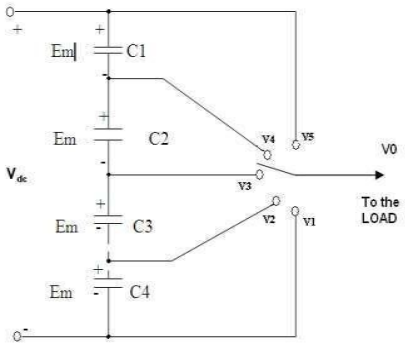
Fig1.2 Conventional Cascaded Multilevel Inverter.[2]

2]Vinayaka B.C, S.Nagendra Prasad "Modeling and Design of Five Level Cascaded H-Bridge Multilevel Inverter with Dc/Dc Boost Converter" *Vinayaka B.C Int. Journal Of Engineering Research And Applications ISSN: 2248-9622, Vol. 4, Issue 6(Version 5), June 2014,*

Introduction

Multilevel inverters have attracted much attention in high power electronics applications as the solution of needs for higher power ratings and the reduction of the output harmonic distortion, voltage stress (dv/dt) and EMI phenomenon. Multilevel began with the 3-level converter, then several be multilevel converter topologies[5] has been developed. Multi-level inverters provide more than 2 voltage levels. The basic principle of a multilevel inverter is to connect semiconductor switches in series so that the converter can operate with power ratings of several megavolt amperes and at medium voltage levels (1kv to 35kv) that exceed the individual switch voltage ratings. The output voltage waveform will be synthesized from several levels of capacitor voltage sources. As the number of levels increases, the obtained output waveform approaches the sinusoidal wave with less distortion, less switching frequency, higher efficiency etc…

Basic Principle of Operation



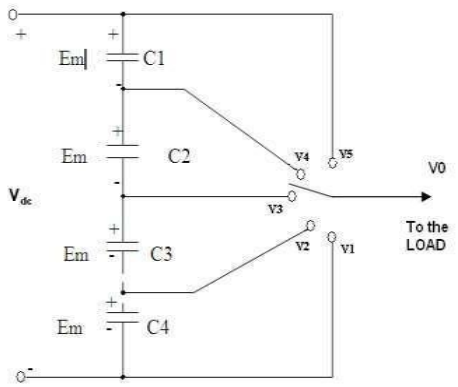


Fig 1.3 Schematic of Multilevel inverter.

Fig 1.3 shows the schematic of a pole in a multilevel inverter where V_O indicates an output phase voltage where any voltage level can be obtained depending on the selection of node voltage V1, V2, etc, hence this pole can be referred as single pole multiple throw switch. Series connected capacitor acts as the energy tank for the inverter, providing some nodes to which the multilevel inverter can be connected by connecting the switch to one node at a time; one can obtain the desired output

Types of multilevel inverters

- Diode-clamped multilevel inverter
- Flying capacitor multilevel inverter
- Z-Source multilevel inverter
- Cascaded multilevel inverter with separate dc sources.

Cascaded Multilevel Inverter

Each single DC sources is associated with a single H-bridge converter & AC terminal voltages of different level converters are connected in series & can generate three different voltage outputs ,+V_{dc}, -Vdc and zero. This is explained with the help of fig 1.4. The AC outputs voltage waveform is the sum of the individual converter outputs. Cascaded multilevel inverter is having a unique and attractive topology such as simplicity in structure, usage of less number of components etc. Their main advantage is that they can generate output voltages with extremely low distortion and lower voltage stresses (dv/dt). They can operate with a lower switching frequency. Cascaded Multilevel Inverter[6] consist of series of H-bridge (Full Bridge) Inverter units. Each bridge will be fed from a separate DC source which may be obtained from batteries, fuel cells, or solar cells. The function of this multilevel inverter is to produce a desired voltage from several Separate Dc Sources (SDCSs).The ac terminal voltages of different level inverters are connected in series. This inverter does not require voltage-clamping diodes or voltage-balancing capacitors unlike in the diode-clamp or flying-capacitors inverter, hence inverter has more advantages. Each inverter level can generate three different voltage outputs +V_{dc}, 0, and −V_{dc} by connecting the dc source to the ac output by different combinations of the four switches, S1, S2, S3, and S4.To obtain +V_{dc}, switches S1 and S4 are turned on whereas −V_{dc} can be obtained by turning on switches S2 and S3. By turning on S1 and S2 or S3 and S4, the output voltage is 0. The ac outputs of each of the different full-bridge inverter levels are connected in series so that the generated voltage waveform will be the sum of all the inverter output voltages.

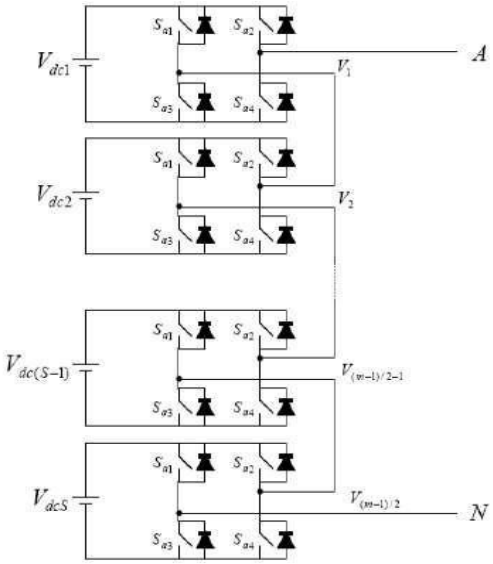


Fig 1.4 Cascaded Multilevel inverter

Cascaded Multilevel Inverter consist of series of H-bridge (Full Bridge) Inverter units. Each bridge will be fed from a separate DC source which may be obtained from batteries, fuel cells, or solar cells. The function of this multilevel inverter is to produce a desired voltage from several Separate Dc Sources (SDCSs).The ac terminal voltages of different level inverters[6] are connected in series. This inverter does not require voltage- clamping diodes or voltage-balancing capacitors unlike in the diode-clamp or flying-capacitors inverter hence inverter has more advantages than other two types.

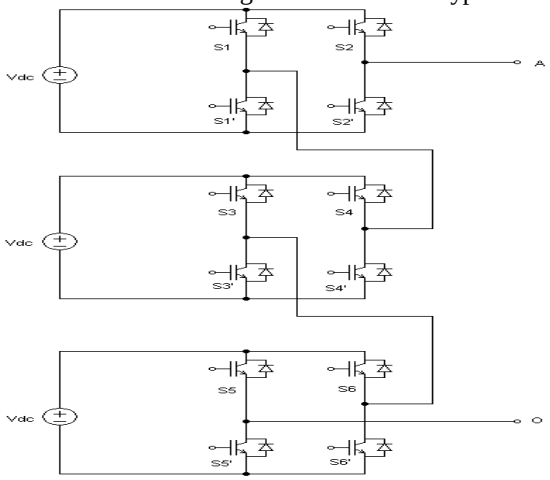


Fig 1.5 Conventional 7 Level Cascaded Multilevel Inverter

Mode of Operation

The Seven Level Cascaded Multilevel Inverter has seven mode of operation and they are as follows

1. Mode 0($0V_{dc}$)
2. Mode 1($1V_{dc}$)
3. Mode 2($2V_{dc}$)
4. Mode 3($3V_{dc}$)
5. Mode 4($-1V_{dc}$)
6. Mode 5($-2V_{dc}$)
7. Mode 6($-3V_{dc}$)

DESIGN AND SIMULATION OF ELECTRICAL CIRCUIT

In designing and simulation of electrical circuit there are 3 steps:

- B u i l d i n g electrical circuit with power library.
- Interfacing of electrical circuit with simulink.
- Measuring voltages and currents.

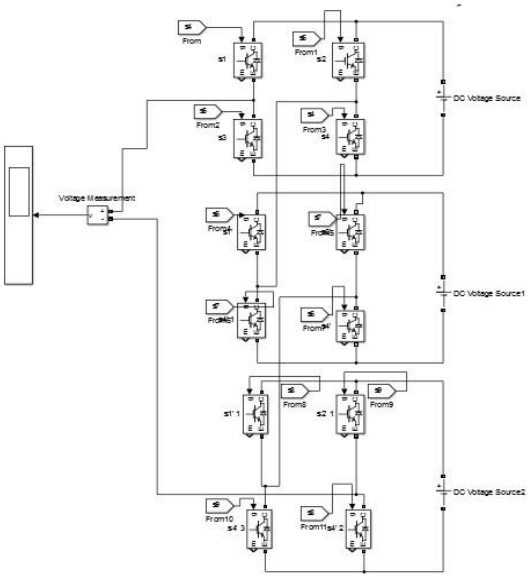


Fig 1.6 Simulation model of the single phase existing topology 5- level cascaded multilevel inverter.

The simulation model[8] of the single phase existing topology cascaded multilevel is shown in figure 1.6.The parameters of various stages of this simulation are:

- Supply voltage = 50V (DC).
- Load =10KΩ.
- Output voltage peak to peak= ±100V (AC).
- Operating frequency=50Hz.
- MOSFET and internal diode are in parallel with a series R circuit. When the gate is supplied, MOSFET conducts and acts as resistance Ron.
- Logical parameters: AND Operator, NOR Operator.

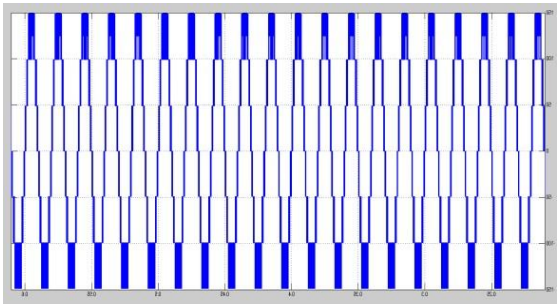


Fig 1.7 Waveforms for Single Phase Existing Topology 5- Level Cascaded Multilevel Inverter.

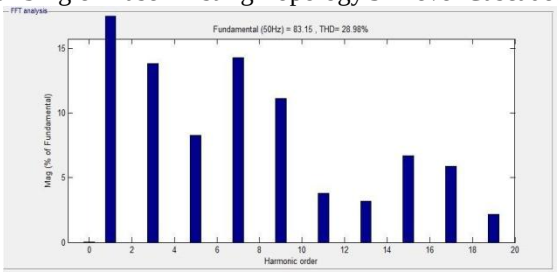


Fig 1.8 represents the total harmonic distortion (%) of the single phase existing topology

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